REMARKS

This is a response to the Office Action mailed November 16, 2004. The Office Action objected to the figures and the specification, rejected claims 1-9, 11, 13-26 under 35 U.S.C. §102, and rejected claims 10 and 12 under 35 U.S.C. §103(a).

Claims 1-6, 8-9, 11, and 15-22 have been amended. Claims 7, 10, 13, 14, 25, and 26 have been cancelled. Claims 27-32 have been added. Claims 1-6, 8-9, 11-12, 15-24, and 27-32 remain pending in this application.

Reconsideration in light of the amendments and remarks made herein is respectfully requested.

In the Drawings

The Office Action objected to the figures because the reference character 508 is mentioned in the description (page 14, line 8) but is not referenced in the figures. Applicants herewith submit Replacement Figure 5 to correct this problem.

Applicants also submits annotated marked-up versions of all changes made to the figures in the present and previous amendments in compliance with the 37 CFR 1.121(d).

Rejections Under 35 U.S.C. § 102

The Office Action rejected claims 1-6, 8, 9, 11, 13, and 14 under 35 U.S.C. §102(b) as being anticipated by Kelly et al. (U.S. Pat. No. 5,798,567) ("Kelly").

Applicants traverse this rejection in its entirety.

Applicants' attorney held an interview with Examiner Chu and her supervisor on Wednesday, January 19, 2005 to discuss the differences between the present invention and the

cited prior art Kelly et al. and Li et al. During this interview Applicants' attorney and Examiner identified differences between Applicants' invention and the prior art.

To more clearly claim the differences between the present invention and the prior art, Applicants have amended several of the claims to clarify the novel aspects of the present claimed invention.

As to claims 1 and 9, Kelly fails to teach or suggest "the substrate having a coefficient of expansion that matches a coefficient of expansion of the memory die to within six parts per million per degree Celsius or less, wherein the second surface of the memory die remains completely exposed." Applicants submit that Kelly fails also to teach or suggest that the substrate 43 has a coefficient of expansion that matches a coefficient of expansion of the memory die (integrated circuit 41) to within six parts per million per degree Celsius or less. Note that one of the novel aspects of the present invention is the discovery of materials that are suitable for substrates yet provide matching thermal expansion coefficients that reduce thermal cracking. Kelly simply fails to teach the type of substrate materials that can be used to achieve this result or the relationship between thermal expansion coefficients of the substrate and memory die as claimed.

Moreover, as to claim 1, Kelly also fails to teach a configuration where the second surface of the memory die remains completely exposed. In fact, Kelly teaches the need for underfilling material 59 (Fig. 4) to prevent thermal cracking. Because of the novel configuration employed by the present claimed invention, it does not need such underfilling and provides improved heat dissipation to the memory die by having the second surface completely exposed. Having the second surface of the memory die exposed improves cooling of the memory die.

As to claims 2 and 11, Kelly also fails to teach or suggest "electrically conductive traces on the first surface to electrically couple at least one solder ball to the memory die directly." In particular, Kelly fails to disclose a direct electrical path (along a single surface of the substrate) between a solder ball and the memory die. As claimed, the solder balls and the memory die are mounted on the same surface of the substrate. The electrical paths taught by Kelly are all indirect, requiring vias (55 in Fig. 4 and 75 in Fig. 5) from a first surface of the substrate to a second surface of the substrate to create an electrical path from a solder ball 49 to the device (41 in Fig. 4 and 61 in Fig. 5). This is a patentable structural difference from what is presently claimed. The present claims requires the electrical path to be a direct path, along a single surface of the substrate as illustrated in Fig. 7 from solder ball 711 to underside coupling 702. It is this type of electrical path that permits the claimed routing scheme as well as the compact size of the chip-scale packages.

As to claim 4, Kelly fails to teach "five sides of the memory die are completely exposed and the first surface of the memory device is substantially exposed for improved heat dissipation." In particular, Kelly requires underfilling 59 that inhibits heat dissipation from the integrated circuit 41. Stacked configurations of chip-scale packages can often cause heat accumulation problems and having greater heat dissipation is very desirable. The novel structure of the present claimed invention enables this to happen.

As to independent claim 5, Kelly also fails to teach or suggest "a staggered routing scheme which, when a plurality of chip-scale packages is stacked together, causes a solder ball of a first chip-scale package to be uniquely electrically coupled with an electrical conductor of a semiconductor device mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two." This claimed limitation is illustrated in Figure

8 of the present application. Kelly does not teach or suggest that its modules can be stacked at all. If fact, the routing scheme disclosed by Kelly would prevent forming an electrical path from a first module to a second module in a stack.

As to dependent claim 8, the Office Action states that Kelly teaches "the combined distance that an electrical component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate." Applicants submit that Kelly fails to teach this physical relation between the claimed components. It is important to note that the spacing between substrates is determined by the height of the solder balls and pads to permit an electrical component and semiconductor device to fit between substrates. Kelly fails to teach the relationship between the substrate spacing and the electrical component and semiconductor device as claimed.

For all of the reasons discussed above, Applicants respectfully request that the Examiner withdraw the rejection of claims 1-6, 8, 9, and 11, under 35 U.S.C. §102(b) as being anticipated by Kelly et al. (U.S. Pat. No. 5,798,567).

The Office Action also rejected claims 1-9, 11, and 13-26 under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Pat. No. 6,597,062) ("Li").

Applicants traverse this rejection in its entirety.

Applicants submit that Li does not teach a chip-scale package architecture as claimed. Li teaches memory modules which are distinct from chip-scale packages. The memory modules 50 are much larger than chip-scale pages. The memory modules 50 of Li include semiconductor devices 54a (Fig. 2b) that may have chip-scale packages inside. However, the Office Action

discusses the memory modules 50 as being the chip-scale packages. This is an incorrect reading of what Li actually discloses.

In the present claimed invention the chip-scale package 100 or 700 is what would be enclosed by each of the semiconductor devices 54a (Fig. 2b) of Li. Chip-scale packages are understood in the art to be much smaller than the memory modules on which they are typically mounted. It is clear that Li teaches a memory module (e.g., the size of a SIMM or DIMM) approximately 2.2 inches by 1.1 inches. (Col. 4, lines 27-34). The present claimed invention, on the other hand, refers to chip-scale packages which are in the order of 10 mm by 12 mm in size. Whatever characteristic Li may disclose for its memory module is not applicable to the much smaller chip-scale packages claimed since the claimed features address problems in increasing the density of die-sized devices. Thus, Applicants submit that Li should be withdrawn as a prior art reference since it is not addressing the same technology or problems as the present claimed chip-scale package invention.

Moreover, even if Li was asserted against the present claims, it fails to teach the limitations claimed.

As to claims 1-6, 8, 9, and 11, Li fails to teach or suggest any of the claimed limitations discussed above with reference to Kelly. In particular, Li fails to teach: (1) the specific relationship between the thermal coefficients of the substrate and semiconductor device, (2) the claimed routing schemes as claimed, (3) and that all chip-scale packages in a stacked configuration have identical routing traces.

As to independent claims 15 and 20, Li fails to teach a routing scheme having "identical routing traces at every level" of a chip-scale package stack. Applicants submit that Fig. 3b of Li

does not teach identical routing traces on each of the stacked configurations. A close study of Fig. 3b indicates that the routing traces on 51a, 51b, and 82 are different from each other. Thus, Li fails to teach this important limitation that reduces the cost of making a stacked assembly in the present invention since every level of the stack is identical. Li's configuration requires a different module 82 since its routing scheme does not permit having the same modules at every level. This tends to increase the costs of making such stacks. The novel routing scheme of the present claimed invention enables a cost-efficient way to form stacks of the same chip-scale packages without a need for special or different routing layer.

As to claims 16 and 21, Li fails to teach that "the substrate has a coefficient of expansion that substantially matches a coefficient of expansion of the memory semiconductor die to within six parts per million per degree Celsius or less" and that "five sides of the memory semiconductor die are completely exposed and a sixth side of the memory semiconductor die is substantially exposed for improved heat dissipation." Note that since Li only teaches memory modules, not chip-scale packages, it fails to teach the claimed relationship between coefficients of expansion. Additionally, it appears that the semiconductor device 54a in Li are surface mounted on the substrate 52. This does not conform to the claims that require five sides of a die to be completely exposed and a sixth side to be substantially exposed for improved heat dissipation. (See Figs. 1 and 3 of the present application for examples).

As to dependent claims 18 and 22, Li fails to teach "the staggered routing scheme forms an electrical path from a first chip-scale package of a first stack that moves inward toward the memory semiconductor die mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two, as the electrical path moves up through each layer of the first stack." Applicants submit that Figs. 3a and 3b of Li do not teach the

claimed staggered routing scheme moves inward at each level as of a stack as claimed and illustrated in Figures 3 and 7 (see references 711, 713, 717, and 719). In particular, Li et al. Fig. 3a does not teach any routing scheme and Fig. 3b only teaches a single trace (84), not a staggered routing scheme as claimed.

As to dependent claim 19, Li fails to teach that "the staggered routing scheme is stepped as it moves up the plurality of chip-scaled packages of a stacked configuration." Instead, Li routing configuration seems to wind from one end to the other as it makes its way up a stack of modules. This is not the same as the claimed stepped routing scheme that permits having the same chip-scaled package at every level of a stack.

Applicants respectfully request that the Examiner withdraw the rejection of claims 1-9, 11, and 15-24 under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Pat. No. 6,597,062).

Applicants also note that the limitations in newly added claims 27-32 are also not taught or suggested by either Kelly or Li. For example, claim 32 claims a routing scheme where "the electrical path moves from the first chip-scale package of a stacked configuration to a last chip-scale package of the stacked configuration along one side of the stacked configuration." This is illustrated in Fig. 8 of the present application as the path for Clock D, for example.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited. Authorization is hereby given to charge our Deposit Account No. 19-2040 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,

Sheldon & Mak PC

I hereby certify that this document is being deposited on February 10, 2005 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313

By: Jennifer Hargis

Signature

Dated: February 10, 2005

Julio Loza
Registration. No. 47,758
SHELDON & MAK
225 S. Lake Ave., 9th Floor
Pasadena, CA 91101
Telephone: (626) 796-4000